Testing the Limits of Power

A Methodology for Measuring the Power Consumption of Indoor-Outdoor Tracking GPS Receivers

All GPS receivers are not created equal — especially in matters of power requirements. Receiver design, operating environment, and intended applications can produce widely varying effects on battery life. An engineering team describes the factors affecting receiver performance and how to measure the consequences for power consumption.

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Personal navigation devices, portable vehicle navigation devices, portable telematics units, GPS-enabled cell phones, GPS-equipped PDAs, portable tracking devices . . . mobile devices for positioning, navigation and communications are proliferating at a fantastic rate. Often these are multi-function devices, perhaps combining an MP3 player, digital camera, cellular modem, *and* a GPS receiver. Although they vary in configuration and functionality, these products all have one thing in common: They rely on batteries to operate. And sooner or later (too often sooner), they inevitably run out of power.

Until the ever-charge battery comes along, we'll have to maximize the field lives of the batteries we do have. One way to do that is to specify energy-saving components when designing these mobile devices, which requires an understanding of how these components work in real-world environments and situations. For an MP3 player or digital camera, power consumption is fairly predictable. For a GPS receiver, however, it is not.

Users operate GPS receivers in a variety of environments, from open sky to closed car trunks, from underground garages to upper-story offices, from beltways to belts. And when they are challenged to find the GPS satellite signal, they use power — sometimes lots of power. That means shorter battery life and a shorter mission life for a GPS-equipped mobile device. Therefore, specifying the best, most power-efficient GPS receiver for a particular application becomes critical. This article proposes a methodology for evaluating GPS receiver chipsets to ascertain their true power consumption in common use scenarios and thus help design engineers pick the right GPS chipset for the job.

Creating a Test Plan

In making design decisions regarding which particular GPS receiver chipset or module to employ, we can fairly easily assess the candidate products based on the navigation solution accuracy required, form factor, and cost. However, comparisons of power consumption among various GPS receiver products are difficult.

Data sheet values provided by the manufacturers are about all that is available to help designers in the selection process. But do those data tell the whole story? A product designer evaluating his or her choices must be careful in interpreting and comparing the power levels quoted in data sheets: for instance, whether the values are presented for full-up GPS solution or for RF front-end or the GPS engine only. Furthermore, we know that certain GPS receiver functions draw more power than others — for example, continuous search mode in a satellite-obscured environment will zap power rapidly, while open sky sampling will not. So how do we go about assessing power consumption and characterizing the energy use of competing GPS receivers? Why, establish a test methodology and procedure, of course!

This article discusses a methodology created for independently assessing GPS receiver chipsets under a variety of environmental scenarios and under different operating modes. If we can devise test methods that designers can apply across different kinds of receiver chipsets, the methodology can provide insight into relative power consumption among the different devices, helping product engineers specify the optimum GPS receiver for their application.

A Powerful Need to Know

In assessing GPS receiver performance, issues of navigation accuracy, time to first fix (TTFF), and ability to acquire GPS signals in degraded urban canyon or indoor environments have been and continue to be important. These very parameters were addressed in Engenex Technologies' 2005 study, "High-Sensitivity/Assisted GPS Receiver Performance Analysis Report," which is the impetus for this power-consumption testing methodology. (See sidebar on page 37, "Myths and Realities of Anywhere GPS.") The move toward integration with mobile computing devices (PDAs, cell phones, laptops) introduced a new shift in the design considerations, however.

Historically, architecture development of integrated GPS capability focused primarily on navigation and performance accuracy, and cost metrics. As portability and mobile computing have proliferated — coupled with a growing demand for location-based services and information — so has the need for better performance at lower power.

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Our goal is to define a medium-grain examination of comparative power performance that will aid in the assessment of both overall average battery consumption as well as component-level measurements.

Clearly, power consumption must be a consideration in the architectural design and component specification process, for several reasons. First, mobile computing devices with embedded GPS are not necessarily tethered and, hence, may need to draw all power solely from an onboard power source. Maximizing battery life, thus extending the field life and mobility of these products, requires designers to minimize the times that batteries must be replaced or recharged.

A second consideration appears as weight and form factors come into play. Consumer electronics products must be attractive and appealing, which often translates into sleek-looking and slim packages. Moreover, they must not hinder natural movements or cause undue burden on the user. Finally, reduced power consumption is associated with a reduction in heat produced by the system, which can also affect overall performance in multi-function mobile products.

To specify the optimum GPS receiver for the device and its application, the specifications engineer/product designer must know not only the positioning and navigation performance characteristics, form factor, and cost, but also the power requirements and anticipated power performance of the receiver in real-world use scenarios.

The Challenge of Variety

The major challenge to benchmarking power consumption in an integrated mobile computing/GPS system is that hardware and software (both user interface and embedded software) vary markedly from platform to platform. Unlike fixed asset computers, no uniform operating system or language is used across all platforms. Differences in user interface and functionality also vary greatly, making it difficult to establish a common baseline of human behavior with which to simulate use of the devices under testing.

As a result of the market-driven push towards a smaller product footprint, the level of integration of the GPS chipset into the computing device may also vary. Although some devices are merely placed in the same box, other implementations will involve chipsets integrated into a multi-layer circuit board and coupled into a system's power management function.

On the surface, power consumption of an integrated device can be assessed at different levels. Extremely course-grain measurements, such as overall battery

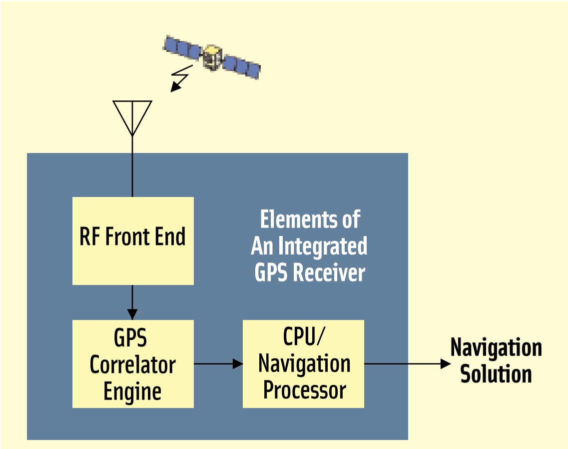

FIGURE 1 Elements of an integrated GPS receiver that will consume power

usage and available time of operation under various user scenarios, provide one level of measurement. Finer-grained looks would involve analysis of the individual component under a variety of scenarios.

However, data sheets and system specs created by the chipset manufacturer usually do not detail the testing methodology that was used. Due to proprietary concerns, vendors ordinarily do not usually offer more than vague details about the various power saving strategies that may be employed.

These factors drive a need to develop a common methodology to assess power consumption across various platforms. Our goal, then, is to define a medium-grain examination of comparative power performance that will aid in the assessment of both overall average battery consumption as well as component-level measurements coupled with specific use cases and functionality.

Receiver Architecture: Comparing Platforms

In assessing the state of the art of low power/high sensitivity GPS receivers, we discover that definitions of low power, very low power, and even ultra low power vary widely throughout the industry; a common standard does not appear to exist. Exactly which pieces of the overall GPS platform are being analyzed in manufacturers' statements on power performance can create an additional point of confusion.

As shown in **Figure 1** an integrated GPS solution consists of, at a minimum, an RF front-end section that down-converts and digitally samples the GPS signals, and a GPS engine which performs correlation and contains the delay and phase lock loops that implement signal tracking. Additionally, the navigation algorithms that convert the raw GPS data and satellite orbits into a navigation and timing solution must reside in a central processing unit (CPU) that is either integrated with the GPS engine or operated separately.

So, power consumption values may refer to the RF front end, the GPS engine, or a combination of these two, which may or may not be coupled with the CPU functions to perform navigation. Except in cases where snapshots of raw uncorrelated data may be sampled and sent across a network connection for subsequent processing, a navigation solution is the goal of a GPS implementation. Therefore, our methodology only addresses integrated solutions capable of performing all three functions.

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Power consumption goes up dramatically when the GPS receiver is searching for satellites or attempting to correlate to very weak signals.

Apples and Oranges

Product comparisons are complicated by differences between evaluation kits provided by chipset manufacturers and designers' actual plans for chipset integration. For example, evaluation kits provided by some manufacturers are intended to enable a demonstration and evaluation of the receiver's ability to acquire and track GPS signals in weak-signal, degraded environments. In such kits the software interfaces are generally PC implementations with communication across a USB or serial interface, and little thought may be given to minimizing power consumption.

This will not affect testing of power consumption during full-up search mode or tracking in open sky environments, but it could be crucial for comparing the ability to track for short periods then return to sleep. Test methodology should include a careful analysis of time to first fix (TTFF) to augment the testing of power consumption during all-out search mode and provide insight into how well the receiver may perform in its intended application.

Power-Saving Techniques

Most modern GPS chipsets designed for low power consumption achieve this in part with the use of the latest silicon germanium and BiCMOS technologies. Coupled with a small form factor to reduce loss due to the physical size of the components, these enable the use of 3.3 volt logic.

When these hardware and form factor power-saving techniques are combined with assisted GPS to enable rapid TTFF, along with power-saving sleep modes, significant improvements can be expected. These may be called trickle power mode, sleep, standby, doze, or similar terms by different manufacturers, but they are generally implemented in a similar fashion across different platforms.

In general, power consumption goes up dramatically when the GPS receiver is searching for satellites or attempting to correlate to very weak signals. This active state consumes the highest level of power. In a sleep or standby mode the RF front end and GPS engine are powered down, and only the CPU processor is enabled.

Upon manual initialization or reception of a real-time clock signal, the CPU will activate the RF and GPS circuitry. In more dramatic attempts to save power, some designs will implement a deeper sleep mode in which even the CPU is powered down.

To save power when repowering the GPS subsections of the integrated device, reaching a state that will enable acquisition of GPS signals and a navigation fix as quickly as possible is critical, after which the device will then again be powered down. This can be achieved with various aiding technologies that preposition the correlators to aid in rapid acquisition of the GPS signals.

Depending on the implementation, this may involve the storage of GPS ephemerides or Doppler/orbit state information and clock state (or even attempts to keep the oscillator at a steady state to minimize clock errors). Other systems will rely on an external network connection to supply these data to the GPS receiver engine upon power up. However it is accomplished, the goal is to enable the receiver to perform signal acquisition and navigation fixes as rapidly as possible before returning to the "hibernate" state.

Having defined what we will test, let's look at how we test them.

Myths and Realities of Anywhere GPS: High Sensitivity vs. Assisted Techniques

The work study discussed in this article is a follow-on to an earlier research effort. In that study, six GPS high-sensitivity assisted GPS (AGPS) chipsets were compared against each other for accuracy and performance in a variety of real-world environments. The conclusions of that study are summarized below.

1. AGPS testing can be done in a variety of ways. AGPS assistance can be supplied via user plane or control plane, but that does not affect chipset selection. The use of assistance can result in much faster acquisition of weaker signals and can facilitate navigation solutions that would not otherwise be possible. The benefit of the time assistance is dependent in a complicated way but extremely important in the system design. In the user equipment design, interference issues need to be carefully considered, as well as time transfer and maintaining time accuracy. The results of our study show that the performance of AGPS devices and high-sensitivity GPS devices can be very close in difficult environments.

2. Our evaluation showed that AGPS performance has a place when integrated with wireless networks to clearly benefit the overall fix yield and consistency. The AGPS receivers under consideration all make use of some conditioning of frequency and time. Our results showed that many applications achieve acceptable results with high-sensitivity (HS) GPS receivers. The new generation of HS GPS receivers, especially those with an ability to implement user plane assistance, should be analyzed for augmented performance only if the application requires improvement in the consistency and yield of the fixes for a very short sampling interval.

3. All the receivers tracked well in the residential and urban environments. Only three receivers were effective in the extreme environments, where degraded receiver performance was the norm. For these three, it was difficult to find environments where the receiver could not at least correlate. These results showed that an analysis of AGPS receiver level performance can be done by using a system level test. We also determined that using the actual wireless delivery mechanism does not test AGPS or HS GPS, rather it tests latency.

4. Accuracy and power consumption are the parameters most often being measured and advertised as necessary to evaluate AGPS or HS receivers; in fact, these parameters didn't directly correlate with the best sensitivity results.

5. Because of the large variation in startup times and current draw during that time on all the receivers, one cannot simply use current statistics to select an ideal receiver. The HS GPS receiver could not outperform the AGPS receiver on power even though the HS GPS receiver had a current draw in the navigation mode that was 50 percent less than the AGPS receiver.

Measurement Methodology

At the initial consideration, the concept of measuring the GPS power consumption would seem to be a straightforward process: simply measure the current flow, and the voltage and power equals voltage multiplied by the current. However, providing a common criterion for measuring the power consumption of a variety of GPS receivers is actually a little tougher than that. Successfully generating valid comparisons ideally requires as repeatable a set of power consumption measurement conditions as possible.

For example, measurement of current typically involves the serial introduction of a shunt resistance, of a known value, on the power lead and then the measurement of the voltage drop across the resistor. Because modern GPS receivers have been designed to minimize their power consumption, the range of currents that need to be measured are on the order of less than 200 milliamperes (mA), and the voltage that needs to be supplied to the receiver is 3.3 v. Thus, the maximum power consumption will be less than 660 milliwatts (mW).

The measurement of the voltage is simple because modern voltmeters use high impedance input of several megohms, which does not affect the available voltage. However, if a conventional series shunt resistor is used for current measurement, the more current that the receiver draws the more the supply voltage to the receiver will drop and have a negative impact upon the receiver's function, and that is precisely what we need to measure.

Fortunately, specialized devices are available that exploit the Hall Effect to detect the magnetic field caused by the current flow. These eliminate the need for a shunt resistor so that no impact occurs on the voltage actually available to the receiver under test. The sensitivity of these Hall Effect devices is approximately 500 mV per ampere, and the

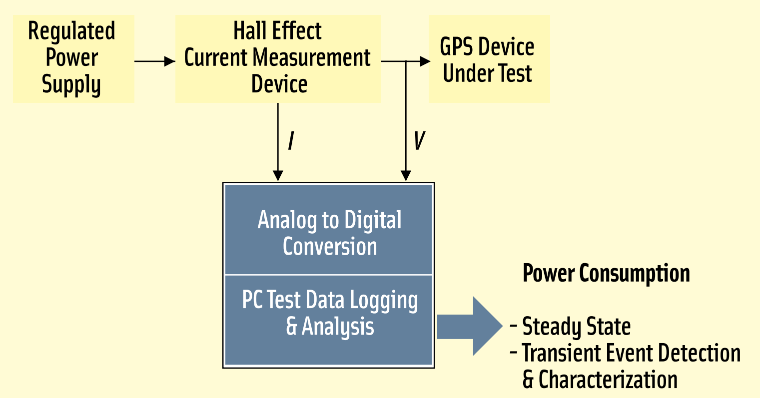

FIGURE 2 Setup for Power Consumption Measurements.

Receiver	SW/ FW/HW versions	Specified Power Consumption (Full Power)	TTFF (Hot Start)
SiRF Star III	tbd	60 mW	1 sec
GlobalLocate	tbd	Not specd	1 sec
QinetiQ	tbd	60 mW	1 sec
u-blox	tbd	70 mW	3 sec
uNav	tbd	50 mW	2 sec
NemeriX	tbd	25 mW	1 sec

TABLE 1. Candidate Receivers for Testing

device has an accuracy of 1 mA, making our power measurement accuracy approximately 3 mW.

This Hall Effect current measurement implementation also provides very high sampling rates (up to 100 kHz). A high sampling rate enables the detection of receiver-imposed current-surge transient events, as the receiver switches its acquisition modes. The existence of current surges is important to know because they can cause sudden voltage changes on the host device power bus, which can be very disruptive to high-speed digital operations of the host device into which a GPS chipset is integrated.

Each benchmark test should be conducted using a regulated power supply, rather than batteries, because battery voltage may change over time. That, in turn, transforms the voltage metric into a variable function of total charge, charge history, and environmental history. The basic approach should place an oscilloscope in line with the power supply and then place the receiver into a steady state (either performing snapshot fixes or in search/continuous correlation mode) under the different operating environments.

A basic idea of how this would be done is shown in Figure 2.

As a test of the reasonableness of results, a mathematical calculation can be used to compare power consumption based on manufacturer's specifications for their GPS chipsets in each scenario. This should identify differences and potential issues, such as a device entering a sleep mode and no longer attempting to acquire GPS at all after a given point.

Establishing Benchmarks

Test benchmarks must measure performance in a variety of use cases. In general, an integrated GPS device will not operate continuously, as that would demand extreme levels of power consumption and generally prove unnecessary for most applications. Most devices used in integrated applications attempt to minimize TTFF, which generally requires aiding information —essentially placing the GPS receiver in a hot start mode from a cold start environment. Therefore, if the device can acquire an instantaneous snapshot measurement of GPS data, then turn itself off, its power consumption will be lower.

While it is difficult to assess the specifics of such behavior from outside of the device, the receiver's general performance can be measured and evaluated by placing the device in various degraded or open sky environments. By conducting continuous mode tracking (to assess how quickly battery life will degrade if the device is not capable of tracking) or snapshot tracking over an extended period, with full open sky view, one can assess how the device will perform under normal best-case usage.

Therefore, the test methodology should place receivers in environments representing common-use scenarios:

Open-Sky Mode. We place the receiver in an environment with few or no obstructions, allowing determination of "best" performance. We allow the devices to acquire a full ephemeris set and operate for several minutes so that the receiver's temperature-compensated crystal oscillator and/or other internal systems can stabilize. Next we place the devices into continuous navigation mode and assess power usage. Additional tests can be done, querying the device to produce navigation solutions on fixed intervals: 20 or 30 seconds, for example, over a period of several hours.

Typical Indoor Environment. We repeat the tests with the devices placed in a setting typical of an indoor environment, approximately 7dB down from open-sky mode. This environment will simulate the typical indoor use cases, where navigation is possible and the GPS receiver can still download ephemeris data from the GPS navigation payload.

Anechoic Chamber. Lastly, we conduct tests with the device placed in an anechoic chamber, simulating signal degradation greater than 20 dB below open-sky mode. Under such a scenario, the GPS device will not be able to track GPS signals, and no aiding data will be provided. We expect that this will cause GPS receivers to attempt to acquire satellites and enter a search mode that will aid in assessing the power consumption under cases where GPS is difficult or impossible to acquire. Special emphasis should be placed on determining if each device is actually attempting to acquire GPS during such periods rather than simply turning itself off to save power.

Figure 3 shows typical carrier-to-noise ratios in the various environments planned for these tests.

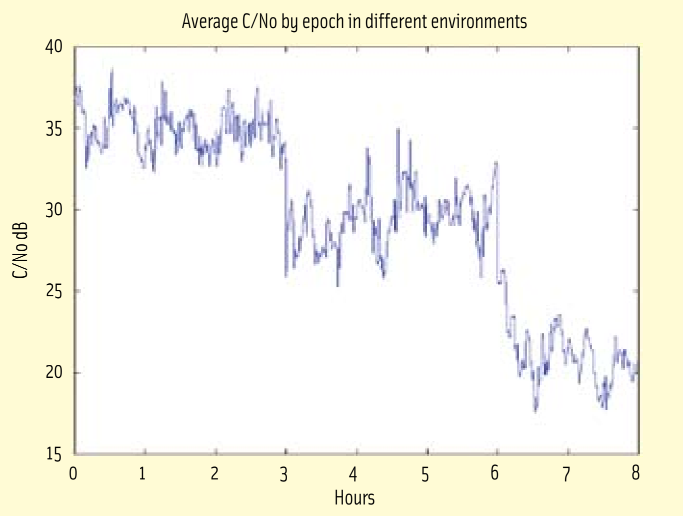

FIGURE 3 Average C/No in various environments- Open Sky, Indoors, Inside Enclosure

that meet these criteria, and for which evaluation kits exist.

For many of the chipset manufacturers, firmware upgrades tend to occur often on the scale of a few months. Software version and hardware version upgrades occur less frequently, but still happen on a regular basis. The latest generation of software and firmware along with current generations of hardware will be used in the testing procedure, as these changes can have significant effects on the ability to track in degraded environments, and on the amount of power consumed.

Receiver	Power Consumption (Search/ Tracking)	Average Hot Start TTFF	Horizontal CEP (m)
RCVR A	25 mW	5 sec	12 m
RCVR B	30 mW	7 sec	23 m
RCVR C	93 mW	8 sec	15 m

TABLE 2. Sample Results Table

Test results will be presented as a function of each environmental scenario (Open Sky Mode, Typical Indoor Environment representing a degraded signal level, and Anechoic Chamber representing no GPS signal), as well as each user mode (continuous tracking/searching or snapshot measurement mode).We expect that direct comparisons of the GPS receivers operating in open sky continuous tracking mode or continuous search mode will be readily achievable.

To assess the power consumption of GPS receivers — assuming that they are fully integrated with all available power-saving modes correctly implemented so that power consumption is minimized — the statistic of time to first fix will be important. Our tests will determine this value for each platform in each mode. Measuring the power consumption of the device in full-up continuous tracking and then relating this to the time required to achieve a navigation solution will provide a look at the best-case scenario for power savings. Additionally, we will assess the accuracy of the produced navigation solutions by performing all testing at a well-surveyed location. Results will be presented in a format consistent with what is shown in Table 2.

The results of such a study should fill a critical gap that now exists in the design process, affording design engineers the ability to select the most appropriate GPS receiver module or chipset for the application. For more information about the study, contact Mike Mathews, michael.mathews@engenex.net.

Testing the Test

This summer (2006) Engenex will apply this newly designed methodology in a study of GPS receiver chipsets. High sensitivity/ low power evaluation kits are available from SiRF, GlobalLocate, QinetiQ, and u-blox. Of these, the GlobalLocate unit is the only one that does not operate off of batteries, but rather relies on the USB port for power. Additionally, integrated chipsets available from uNav and NemeriX will be included in the study.

The candidate receivers to be used in this study are shown in Table 1 with manufacturer specified power, Hot Start TTFF statistics. This list is compiled from a representative sampling of commercially available GPS receivers that have weak signal capability, have low power consumption, and are intended to be integrated with other devices. The actual testing will include all chipsets

Manufacturers

The Sentron CSA-1V Hall Effect current measurement device, **Sentron AG,** Zug, Switzerland, will be used in this scenario. The OMB-DAQ-55/56 Analog to Digital Converter, **Omega Engineering,** Stamford, Connecticut, will be used for data acquisition and power supply voltage and output voltage measurements from the Hall Effect Current Sensor.

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